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REMARKS

- Claims 1-16, and 18-30 remain pending
- Claims 1, 19 and 24 are the only pending independent claims
- Claims 1-4, 6, 13-16, 18-28 are amended; no new matter has been added
- Claim 17 is canceled without prejudice

I. CLAIM REJECTIONS 35 U.S.C. § 102(b)

Claims 1-7, 9, 10, 12-16 and 18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,404,482 ("Stamm"). Applicants respectfully traverse this rejection.

Applicants respectfully submit Stamm does not appear to disclose the all features of the present invention as disclosed in the amended claims. Specifically, Stamm does not appear to show "one or more portions of the control structure are accessed by hardware during a hardware update operation" as recited in Claim 1. In the context of the present invention, it is understood that the term "hardware" as used in the specification refers to a logic device such as an application specific integrated circuit (ASIC). See, for example, Applicants' Specification, Page 6, lines 24-29. This is in contrast to a software driven processor. One of ordinary skill in the art would understand an ASIC to be an integrated circuit (e.g., logic building blocks that can be wired together) customized for a particular use which may incorporate memory blocks including ROM, RAM, EEPROM, or Flash, for example. This "hardware" differs from "a software access" (e.g., instructions executed by a processor) in that the software comprises instructions to be carried out and may

be performed on any number of different processors. See, for example, Applicants' Specification at Page 7, lines 5-14.

The Examiner appears to refer to a processor of Stamm as hardware that may "lock a block of memory to modify the data stored there" (Office Action, Page 2, Section 4A). However, the processors (e.g., CPUs 28 in FIG. 1) of Stamm utilize a system of instructions issued from and executed by the processors to set a lock on a memory block. This appears to show software, not hardware control. See at least Stamm FIG. 7 and Col. 21, lines 15-66. This is in sharp contrast to the invention as claimed.

Despite these distinctions and solely to expedite prosecution, Applicants have amended claims 1-4, 6, 13-16, 18-28 to make explicit what was implicit. Applicants have amended the claims to clarify the claim terms hardware (e.g., "logic device") and software (e.g., "instructions executed by a processor").

Accordingly, Stamm does not appear to show "writing a pointer to a control structure in a hardware update list while one or more portions of the control structure are *accessed by a logic device* during a hardware update operation" (emphasis added) AND "*delaying instructions executed by a processor from accessing the one or more portions of the control structure* during a software update operation while the pointer to the control structure is on the hardware update list" (emphasis added).

Claim 1, as amended, recites, among other things, "one or more portions of the control structure are accessed by a logic device" and "delaying instructions executed by a processor from accessing the one or more portions of the control structure." Independent claims 19 and 24 recite

similar features. Support for these amendments may be found in Applicants' Specification at least at Page 7, lines 5-9 and Page 3, lines 7-10.

According to the method of independent claim 1, the present invention provides for accessing a control structure using "a logic device" (e.g., application specific integrated circuit, locking logic, registers, memory, etc.). See, for example, Applicants' Specification, Page 6, lines 18-29. While this "logic device" is accessing the control structure, a pointer (e.g., "information representing at least a portion of an address of the control block," Applicants' Specification, Page 8, lines 1-3) is written to a hardware update list. While the pointer remains on the hardware update list, "instructions executed by a processor" (e.g., software instructions from processors 106a-N in FIG. 1) are delayed (e.g., temporarily prevented) from accessing the control structure. In other words, the present method provides for a *hardware* logic device accessing (e.g., for a read-write operation) a control block and a method of preventing a *software* update to that control block while the *hardware* is accessing the control block.

In contrast, Stamm describes methods and apparatus wherein "a specified memory block [e.g., a control structure] is locked and unlocked by a READ LOCK--WRITE UNLOCK command sequence *originated by an instruction execution unit in the processor*." (emphasis added) Stamm, Col. 3, lines 54-57. That is, Stamm describes a method in which "instructions executed by a processor" (e.g., *software*) access a control structure, lock the control structure, and prevent other *software* from accessing the control structure. See also Stamm, Col. 5, line 33 to Col. 6, line 44 and associated

FIG. 1. Here, Stamm further describes how processors (e.g., CPUs 28):

> can access the memory 12, and so the blocks of data in the caches 14 or 15 can become obsolete. If a CPU 28 writes to a location in the memory 12 that happens to be duplicated in the cache 15 (or in the primary cache 14), then the data at this location in the cache 15 is no longer valid. For this reason, blocks of data in the caches 14 and 15 are "invalidated" as will be described, when there is a write to memory 12 from a source other than the CPU 10 (such as the other CPUs 28). The cache 14 operates on a "write-through" principle, whereas the cache 15 operates on a "write-back" principle. When the CPU 10 executes a write to a location which happens to be in the primary cache 14, the data is written to this cache 14 and also to the backup cache 15 (and sometimes also to the memory 12, depending upon conditions); this type of operation is "write-through". When the CPU 10 executes a write to a location which is in the backup cache 15, however, the write is not necessarily forwarded to the memory 12, but instead is written back to memory 12 only if another element in the system (such as a CPU 28) needs the data (i.e., tries to access this location in memory), or if the block in the cache is displaced (deallocated) from the cache 15. (Stamm, Col. 6, lines 20-44)

In other words, Stamm describes a system of software access to memory, not "writing a pointer to a control structure in a hardware update list while one or more portions of the control structure are *accessed by a logic device* during a hardware update operation" (emphasis added) as shown in Applicants' Claim 1. Thus, as Stamm does appear not teach or

suggest accessing a control structure with a hardware logic device, the reference cannot anticipate the present invention.

For the above reasons, the Stamm patent does not appear to disclose "writing a pointer to a control structure in a hardware update list while one or more portions of the control structure are accessed by a logic device during a hardware update operation" as recited by independent claim 1. Consequently, Applicants respectfully submit claim 1 is not anticipated by Stamm. Claims 2-7, 9, 10, 12-16 and 18 depend from independent claim 1. Each dependent claim inherits the features of their independent claims and are thus not anticipated by Stamm either. Accordingly, Applicants respectfully request the Examiner reconsider and withdraw the rejection of these claims.

II. CLAIM REJECTIONS 35 U.S.C. § 103(a)

Claims 11, 17, and 19-30 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Stamm. Applicants respectfully traverse this rejection.

Contrary to the Examiner's assertion, as discussed above in reference to independent claim 1, Stamm does not appear to disclose the invention as claimed. Independent claims 19 and 24 recite similar features to those discussed above with reference to claim 1. As Stamm does not appear to disclose all of the claim features, specifically "writing a pointer to a control structure in a hardware update list while one or more portions of the control structure are *accessed by a logic device* during a hardware update operation" (emphasis added) AND "*delaying instructions executed by a processor from accessing the one or more portions of the control structure* during a software update operation while the pointer to the

control structure is on the hardware update list" (emphasis added), the Examiner has failed to provide a *prima facie* case of obviousness.

Further, Stamm is silent as to use in a network processing system (see Office Action, Page 4, line 2) and the Examiner has not provided a reference which discloses the claim features on which the § 103 rejection is based. Still further, the Examiner has not provided anything that suggests the desirability and thus the obviousness of making the combination which is required to make Applicants' invention. Simply stating that "Stamm et al. could be utilized by any system" (Office Action, Page 4, Section A) does not show where in the reference it expressly or impliedly discloses the current invention, because it does not.

Accordingly, as the Examiner has not established a *prima facie* case of obviousness, Applicants respectfully request the Examiner reconsider and withdraw the rejection of independent claims 19 and 24. Dependent claim 11 depends from independent claim 1, discussed above. Dependent claims 20-23 depend from independent claim 19. Dependent claims 25-30 depend from independent claim 24. Each dependent claim inherits the features of their independent claims and are thus not anticipated by Stamm nor are they obvious in view of Stamm. Applicants respectfully request the Examiner reconsider and withdraw the rejection of these claims.

Dependent claim 17 is canceled without prejudice. Applicants note the Examiner has not provided a specific rejection of dependent claim 8, though claim 8 is listed as rejected in the "Disposition of Claims." Applicants respectfully submit that claim 8 is dependent from claim 1 and is allowable for at least the same reasons.

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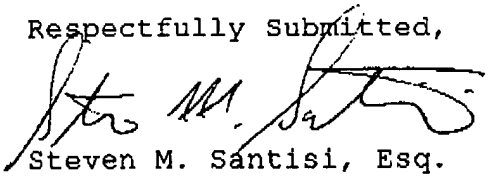
III. CONCLUSION

The Applicants believe all the claims to be in condition for allowance, and respectfully request withdrawal of the objections and issuance of a Notice of Allowance.

Applicants do not believe any fees are due in conjunction with this amendment. However, if an Extension of Time is required to make this response timely, please accept this sentence as such a request and charge Deposit Account No. 04-1696 the requisite fee. Applicants do not believe any other fees are due regarding this amendment. If any other fees are required, however, please charge Deposit Account No. 04-1696. The Applicant encourages the Examiner to telephone Applicant's attorney should any issues remain.

Respectfully Submitted,



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